DATA SHEET

TDA4510
PAL decoder

Product specification
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

GENERAL DESCRIPTION

The TDA4510 is a colour decoder for the PAL standard, which is pin sequent compatible with multistandard decoder TDA4555 and also pin compatible with NTSC decoder TDA4570. It incorporates the following functions:

Chrominance part

- Gain controlled chrominance amplifier with operating point control stage
- Chrominance output stage for driving the 64 µs delay line
- Blanking circuit for the colour burst signal
- Automatic chrominance control (ACC) with sampled rectifier during burst-key

Oscillator and control voltage part

- Reference oscillator for double subcarrier frequency
- Gated phase comparison
- Identification demodulator and automatic colour killer
- Sandcastle pulse detector
- Service switch

Demodulator part

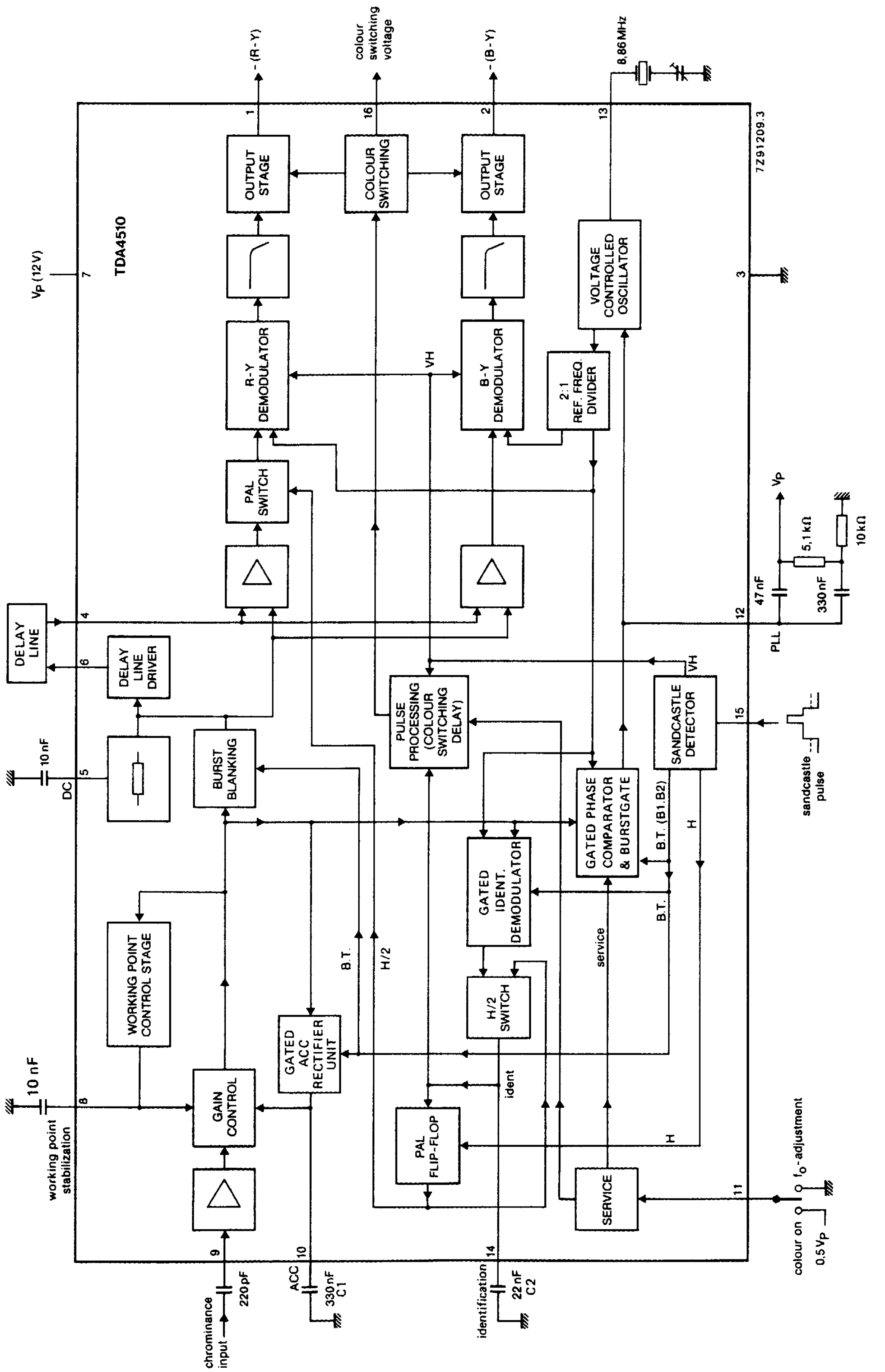
- Two synchronous demodulators for the (B-Y) and (R-Y) signals
- PAL flip-flop and PAL switch
- Colour switching stages
- Separate colour switching output
- (B-Y) and (R-Y) signal output stages
- Internal filtering of residual carrier

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{7-3}$	typ.	12	V
Supply current	$I_P = I_7$	typ.	50	mA
Chrominance input signal (peak-to-peak)	$V_{9-3(p-p)}$		10 to 400	mV
Chrominance output signal (peak-to-peak)	$V_{6-3(p-p)}$	typ.	1,6	V
Colour difference output signals (peak-to-peak values)				
–(R-Y) signal	$V_{1-3(p-p)}$	typ.	1,05 V ± 2	dB
–(B-Y) signal	$V_{2-3(p-p)}$	typ.	1,33 V ± 2	dB
Sandcastle pulse, required amplitude for				
burst gating level	V_{15-3}	typ.	7,7	V
horizontal pulse separation	V_{15-3}	typ.	4,5	V
vertical and horizontal pulse separation	V_{15-3}	typ.	2,5	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38); SOT38-1; 1996 November 26.



External capacitors in Fig.1
C1 filter capacitor for control voltage (pin 10)
C2 filter capacitor for identification signal (pin 14)

Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

DIVIDER STAGES

The divider stages provide –(R-Y) and –(B-Y) reference signals with the correct 90 degrees relation for the demodulators.

PHASE COMPARATOR

The phase comparator compares the –(R-Y) reference signal with the burst pulse and controls the frequency and phase of the reference oscillator.

IDENTIFICATION DEMODULATOR

The identification demodulator delivers a positive going identification signal for PAL-signals at pin 14, also used for the automatic colour-killer.

SERVICE SWITCH

The service switch has two functions. The first position ($V_{14-3} < 1$ V) allows the adjustment of the reference oscillator. Therefore the colour is switched on and the burst for the oscillator PLL is switched off. The second position ($V_{14-3} > 5$ V) switches the colour on and the output signals can be observed.

SANDCASTLE PULSE DETECTOR

Sandcastle pulse detector for burst-gate, line and blanking (horizontal and vertical) pulse detection. The vertical part of the sandcastle pulse is needed for the internal colour-on and colour-off delay.

PULSE PROCESSING PART

Pulse processing part which shall prevent a premature switching on of the colour. The colour-on delay, two or three field periods after identification of the PAL signal, is achieved by a counter. The colour is switched off immediately or at the latest one field period after disappearance of the identification voltage.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	$V_P = V_{7-3}$	10,8 to 13,2		V
Currents				
at pins 1 and 2	$-I_{1,2}$	max.	5	mA
at pin 6	$-I_6$	max.	15	mA
at pin 16	$-I_{16}$	max.	5	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}	–25 to + 150		°C
Operating ambient temperature	T_{amb}	0 to + 70		°C

CHARACTERISTICS

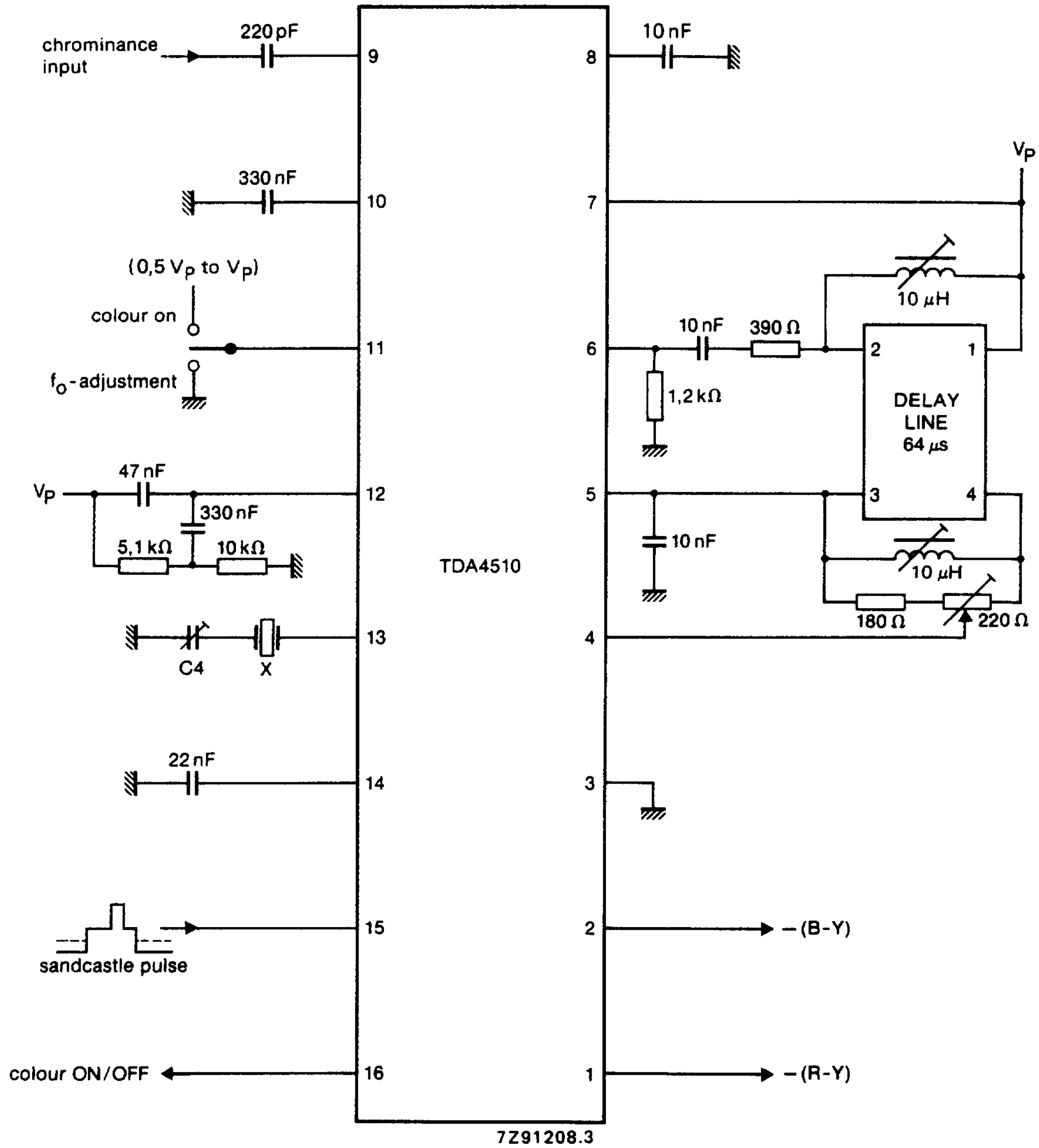
V_P = 12 V; T_{amb} = 25 °C; measured in Fig.2 unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply current	I_7	–	50	–	mA
Chrominance part					
Input voltage range (peak-to-peak value)	$V_{9-3(p-p)}$	10	–	400	mV
Nominal input voltage (peak-to-peak value)					
with 75% colour bar signal	$V_{9-3(p-p)}$	–	100	–	mV
Input impedance	Z_{9-3}	–	3,3	–	kΩ
Input capacitance	C_{9-3}	–	4	–	pF
Colour ON					
Chrominance output voltage (peak-to-peak)					
with 75% colour bar signal	$V_{6-3(p-p)}$	–	1,6	–	V
d.c. voltage at chrominance output	V_{6-3}	–	8,2	–	V
Oscillator and control voltage part					
Oscillator frequency	f_o	–	8,8	–	MHz
Input resistance	R_{13-3}	–	350	–	Ω
Catching range					
(depending on RC-network at pin 12)	f	±400	–	–	Hz
Control voltage					
without burst signal	V_{14-3}	–	6,0	–	V
colour on switching threshold	V_{14-3}	–	6,6	–	V
hysteresis of colour switching	V_{14-3}	–	150	–	mV
flip-flop correction (FFC) voltage	V_{14-3}	–	5,5	–	V
hysteresis of FFC	V_{14-3}	–	170	–	mV
Colour-on delay		2	–	3	f.p.(1)
Colour-off delay		0	–	1	f.p.(1)
First service position (PLL is inactive					
for oscillator adjustment, colour on)	V_{11-3}	0	–	1	V
second service position (colour on)	V_{11-3}	5	–	–	V
Colour switching output (open npn emitter)					
output current	$-I_{16}$	–	–	5	mA
colour-on voltage	V_{16-3}	–	6	–	V
colour-off voltage	V_{16-3}	–	0	–	V

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Demodulator part					
Delayed chrominance input signal (peak-to-peak value) with 75% colour bar signal	$V_{4\text{-}3(p\text{-}p)}$	–	200	–	mV
Colour difference output signals (peak-to-peak value)					
–(R-Y) signal	$V_{1\text{-}3(p\text{-}p)}$	0,84	1,05	1,32	V
–(B-Y) signal	$V_{2\text{-}3(p\text{-}p)}$	1,06	1,33	1,67	V
Ratio of colour difference output signals (R-Y)/(B-Y)	$V_{1\text{-}3}/V_{2\text{-}3}$	0,71	0,79	0,87	V
D.C. voltage at colour difference outputs	$V_{1;\ 2\text{-}3}$	–	7,7	–	V
Residual carrier voltage at colour difference outputs					
1 × subcarrier frequency (4,4 MHz)	$V_{1,2\text{-}3(p\text{-}p)}$	–	–	20	mV
2 × subcarrier frequency (8,8 MHz)	$V_{1,2\text{-}3(p\text{-}p)}$	–	–	20	mV
Sandcastle pulse detector					
Thresholds:					
Field- and line-pulse separation pulse ON	$V_{15\text{-}3}$	1,3	1,6	1,9	V
Required pulse amplitude	$V_{15\text{-}3}$	2,0	2,5	3,0	V
Line pulse separation; pulse ON	$V_{15\text{-}3}$	3,3	3,6	3,9	V
Required pulse amplitude	$V_{15\text{-}3}$	4,1	4,5	4,9	V
Burst pulse separation; pulse ON	$V_{15\text{-}3}$	6,6	7,1	7,6	V
Required pulse amplitude	$V_{15\text{-}3}$	7,7	–	–	V
Input voltage during horizontal scanning	$V_{15\text{-}3}$	–	–	1,1	V
Input current	$-I_{15}$	–	–	100	μA

Note

1. f.p. is shortening for field periods in this case.

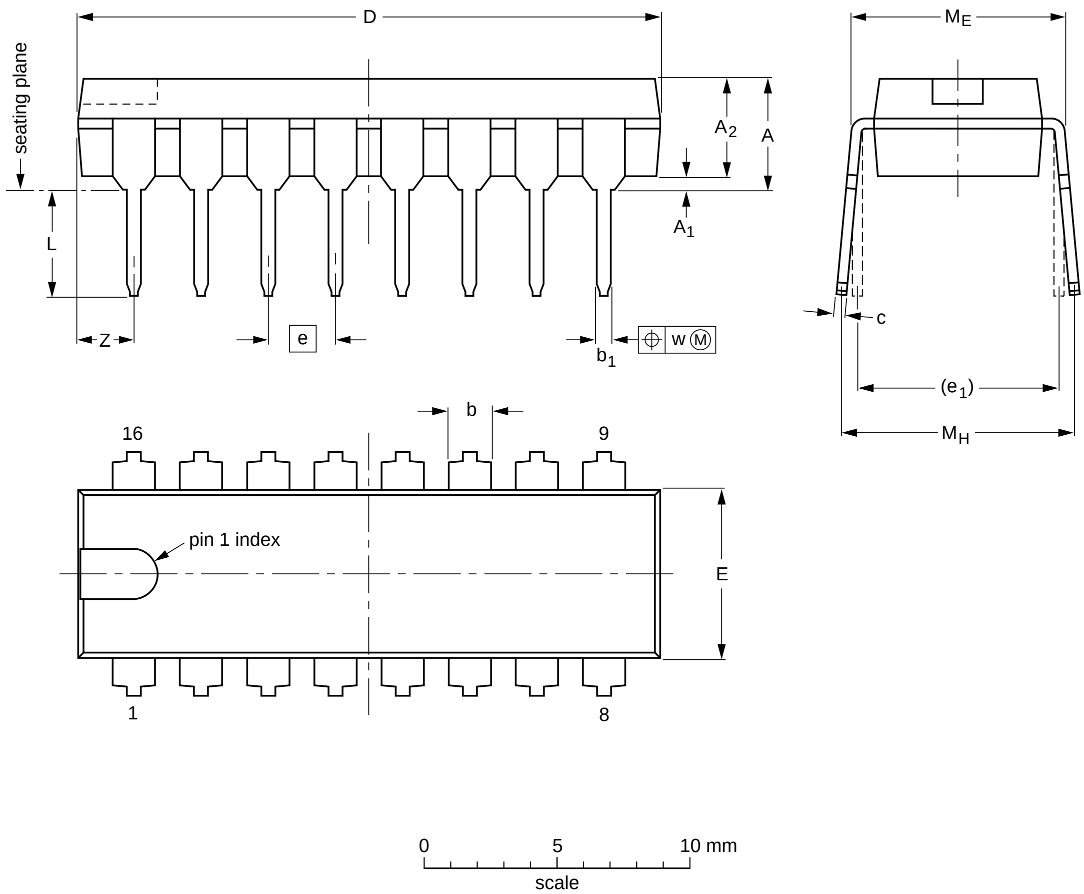


C4 = 5 to 27 pF, X = 8,8 MHz; nominal frequency 8,867 238 MHz; resonance resistance 60 Ω, load capacitance 20 pF, dynamic capacitance 22 fF and static capacitance 5,5 pF.

Fig.2 Application information and test circuit.

PACKAGE OUTLINE

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.